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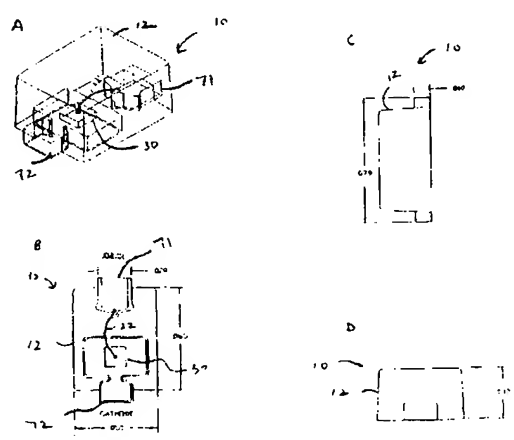
(54) Title: ENCAPSULATED DIE PACKAGE WITH IMPROVED PARASITIC AND THERMAL PERFORMANCE



(57) Abstract: An semiconductor device package (10) with improved thermal properties that limits unwanted parasitics and provides a more consistent distribution of parasitics from one device to another. The package of the present invention (10) is extremely compact and uses, in one embodiment, a minimal length of bond wires (20 and 22) between the terminals (14 and 16) and the attached device (30). The path length of the package (10) is reduced so as to represent only some fraction of a wavelength relative to the terminals (14 and 16) of the package (10). By reducing the length of the bond wires (20 and 22) and selecting the appropriate dielectric constant of the encapsulant (12), the invention provides a package (10) with a unique hexagonal structure that limits the effects of parasitics and provides good thermal dissipation. In a second and third embodiment of the present invention, the semiconductor device package (10) is useful in optoelectronic devices such light emitting diodes with an anode (71) and a cathode (72). The use of the novel design in this implementation also improves thermal properties and limits unwanted parasitics.

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ENCAPSULATED DIE PACKAGE WITH IMPROVED PARASITIC AND THERMAL PERFORMANCE

Cross Reference to Related Applications

This application claims priority of U.S. Provisional Patent Application No. 60/271,940 filed on February 27, 2001 entitled "Encapsulated Die Package with Improved Parasitic and Thermal Performance", and the teachings are incorporated herein by reference.

Technical Field

The present invention relates to an enclosure for a semiconductor device and, more specifically, to an encapsulated molded common leadframe package. More specifically, the invention relates to such a package that limits unwanted parasitics and provides excellent thermal dissipation. The package is useful in three lead devices and two lead devices, including optoelectronic devices such as light emitting diodes.

Background of the Invention

In surface mount assembly, it is common to provide an enclosure or housing for encapsulating a semiconductor device. Currently, numerous package styles are available for surface mount assembly, such as the Standard Outline Transistor 23 (SOT 23), and the Standard Outline Diode 323 (SOD 323). These common leadframe injection molded packages have been used in the industry for many years. However, such package styles suffer from various shortcomings including the existence of parasitics that limit the operating performance of the device past certain high frequencies. With such standard leadframe packages, the

emitting diodes where the encapsulant material is made of a substantially clear, including translucent, epoxy.

Brief Description of the Drawings

For a better understanding of the invention including its features, advantages and specific embodiments, reference is made to the following detailed description along with accompanying drawings in which:

Figure, 1 is a perspective view of a first embodiment of the semiconductor device package of the present invention;

Figure 2 is a top view of a first embodiment of the package, according to the invention, illustrating the arrangement of input/output and ground terminals;

Figure 3 is a side view of a first embodiment of the package of the present invention illustrating the connection of wire bonds from terminal to semiconductor die;

Figure 4 shows an alternate side view of a first embodiment of the package of the present invention;

Figures 5A, 5B and 5C illustrate close-up views of a first embodiment of the package of the present invention with dimensions noted thereon;

Figures 6A, 6B and 6C illustrate close-up views of a first embodiment of the package of the present invention with dimensions noted; and

Figures 7A, 7B, 7C and 7D illustrate close up views of the package according to a second embodiment of the package of the present invention with dimensions noted.

the device 10 is predictable, therefore enhancing the ability of the device 10 to minimize unwanted parasitics as the frequency of operation of signals coupled to the input terminal 14 increases. This enhances the consistency of the package 10 from one device to another. As illustrated in Figure 1, the encapsulant material 12 has taken the form of a hexagonal structure that allows the use of the ground terminal 18 as a shunt comprising the surface where the device 30 is mounted. This surface wraps around the ground terminal 18 essentially at right angles and reaches down to the bottom surface, greatly enhancing the thermal path to ground. This results in overall less thermal capacitance and considerably less thermal resistance.

As is well known in the arts, the power handling capabilities of a semiconductor package depend on how much heat can be dissipated by the device. Too much heat can interfere with the operation of the semiconductor device 30, and as such, heat dissipation is a property of the package 10 that must be controlled accurately. As shown in Figures 2, 5A and 6A, a first embodiment of the package 10 includes conductive leadframe portions in the form of input terminal 14 and output terminal 16 such that power is applied to one side (the input terminal 14) to the device 30 and is output on an opposite side (the output terminal 16). Running approximately orthogonal to the input 14 and output 16 terminals is the ground terminal 18 which provides a shunt extending around the terminal 18, such that the electrical properties of the device 10 are controlled.

Since the bond wires 20 and 22 are kept short, package performance from one device to another is more consistent compared to SOT 23 and SOD 323 type

a mold with one side of the leadframe remaining completely bare copper. Because of the uniqueness of the assembly process, the package 10 allows the thermal path of the die to be outstanding. The full metal bottom allows the heat to transfer directly to a printed circuit board. Leadframe design allows wire bond wires 20, 22 to be extremely short for the package size.

Figures 7A, 7B and 7C illustrate a second embodiment of the present invention for use with two lead devices, including optoelectronic devices such as light emitting diodes. As seen in Figure 7A, if the two lead device is a light emitting diode, then encapsulant material 12 is made of a substantially clear epoxy, with anode 71 and cathode 72. As illustrated therein, the substantially clear encapsulant material 12 has taken the form of a hexagonal structure. The surface of the encapsulant wraps around the anode 71 and cathode 72 and reaches down to the bottom surface, greatly enhancing the thermal path to ground. Further, as can be seen in Figure 7B, the anode 71 and the cathode 72 are positioned opposite to each other, with the cathode 72 further comprising a portion of a conductive lead-frame. The anode 71 has a shaped end surface operable to minimize parasitic capacitance. Alternatively, the cathode 72 could comprise metallization as the means of coupling the cathode 72 to the semiconductor die 30. As seen in Figure 7B, a bond wire 22 couples the anode 71 to the semiconductor die 30. The bond wire 22 could have a length comprising a fraction of the wavelength for which frequency the semiconductor device 70 is designed. The packaged semiconductor device 10 as seen in Figure 7A is adapted for use in an integrated circuit and is advantageously suited for use

embodiments of the present invention. It should be understood that changes to these dimensions can and will occur to those of ordinary skill in the art.

While the invention has been described with regard to specific and illustrative embodiments, this description and the following claims are not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments as well as other embodiments of the invention will become apparent to persons skilled in the art upon reference to the description and is intended that such variations be encompassed and included within the meaning and scope of the following claims.

7. The packaged semiconductor device as recited in Claim 6, wherein the portion of the lead-frame coupled to each of the input terminal(s) and output terminal(s) possess exposed dovetailed side edges operable to allow epoxy to lock on the sides and top of the exposed edges.

8. The packaged semiconductor device as recited in Claim 3, further comprising an end surface of the input terminal(s) being positioned adjacent and parallel to the side surface of the I/O common terminal, and an end surface of the output terminal(s) being positioned adjacent and parallel to the opposing side surface of the I/O common terminal, said end surfaces being shaped so as to minimize parasitic capacitance.

9. The packaged semiconductor device as recited in Claim 8, further comprising a rounded shape on the end surface of the input terminal(s) positioned adjacent and parallel to the side surface of the I/O common terminal, and on the end surface of the output terminal(s) positioned adjacent and parallel to the opposing side surface of the I/O common terminal.

10. The packaged semiconductor device as recited in Claim 8, further comprising length and width dimensions of approximately .079 millimeters and .065 millimeters and a height dimension of approximately .032 millimeters.

11. The packaged semiconductor device as recited in Claim 8, further comprising an operating frequency range from DC to 10 gigahertz.

12. The packaged semiconductor device as recited in Claim 8, further comprising use in a surface mount assembly.

19. The packaged semiconductor device as recited in Claim 1, further comprising a controlled dielectric constant encapsulant operable to provide improved unit-to-unit and run-to-run package parasitic consistency.

20. The packaged semiconductor device as recited in Claim 1, further comprising a light emitting semiconductor as the semiconductor die.

21. The packaged semiconductor device as recited in Claim 20, further comprising a light emitting diode as the light emitting semiconductor.

22. The packaged semiconductor device as recited in Claim 20, further comprising a substantially clear epoxy material as the encapsulant.

23. The packaged semiconductor device as recited in Claim 20, further comprising a cathode and an anode as the plurality of leads.

24. The packaged semiconductor device as recited in Claim 23, further comprising the positioning of the cathode and the anode opposite to each other.

25. The packaged semiconductor device as recited in Claim 24, further comprising an encapsulant with a substantially hexagonal structure around the cathode and the anode essentially at right angles with respect to the substrate.

26. The packaged semiconductor device as recited in Claim 23, further comprising a portion of a conductive lead-frame as the cathode.

27. The packaged semiconductor device as recited in Claim 23, further comprising a shaped end surface of the cathode operable to minimize parasitic capacitance.

28. The packaged semiconductor device as recited in Claim 27, further comprising a rounded shape on the end surface of the cathode.

semiconductor die, a first end of the bond wire being coupled to the anode and a second end of the bond wire being coupled to the semiconductor die.

37. The packaged semiconductor device as recited in Claim 20, further comprising being adapted for use in an integrated circuit.

38. The packaged semiconductor device as recited in Claim 20, further comprising being adapted for use in a surface mount assembly.

39. The packaged semiconductor device as recited in Claim 20, having length and width dimensions of approximately .079 millimeters and .050 millimeters and a height dimension of approximately .032 millimeters.

40. A packaged semiconductor device, comprising:

a light emitting semiconductor, a substrate, an anode, a cathode and an encapsulant material;

the light emitting semiconductor being disposed in the substrate;

a means of coupling the anode to the light emitting semiconductor;

a means of coupling the cathode to the light emitting semiconductor;

a substantially clear encapsulant for encapsulating the light emitting semiconductor, the encapsulant formed of a substantially hexagonal structure around the anode and the cathode with respect to the substrate, the encapsulant material acting as a thermal shunt to ground operable to decrease thermal capacitance and thermal resistance.

41. The packaged semiconductor device as recited in Claim 40, adapted for use in a surface mount assembly.

42. A packaged semiconductor device, comprising:

forming and configuring the encapsulant so as to allow direct dissipation shunting to thermal ground.

46. The method of assembling a semiconductor device package as recited in Claim 45, further comprising shaping the ends of the plurality of leads in a substantially rounded form operable to minimize parasitic capacitance.

47. The method of assembling a semiconductor device package as recited in Claim 45, further comprising a light emitting semiconductor as the semiconductor die.

48. The method of assembling a semiconductor device package as recited in Claim 45, further comprising a cathode and an anode as the plurality of leads.

49. The method of assembling a semiconductor device package as recited in Claim 45, further comprising a substantially clear material as the encapsulant.

50. The method of assembling a semiconductor device package as recited in Claim 45, further comprising the encapsulant having a substantially hexagonal structure essentially at right angles with respect to substrate operable to decrease thermal capacitance and thermal resistance.

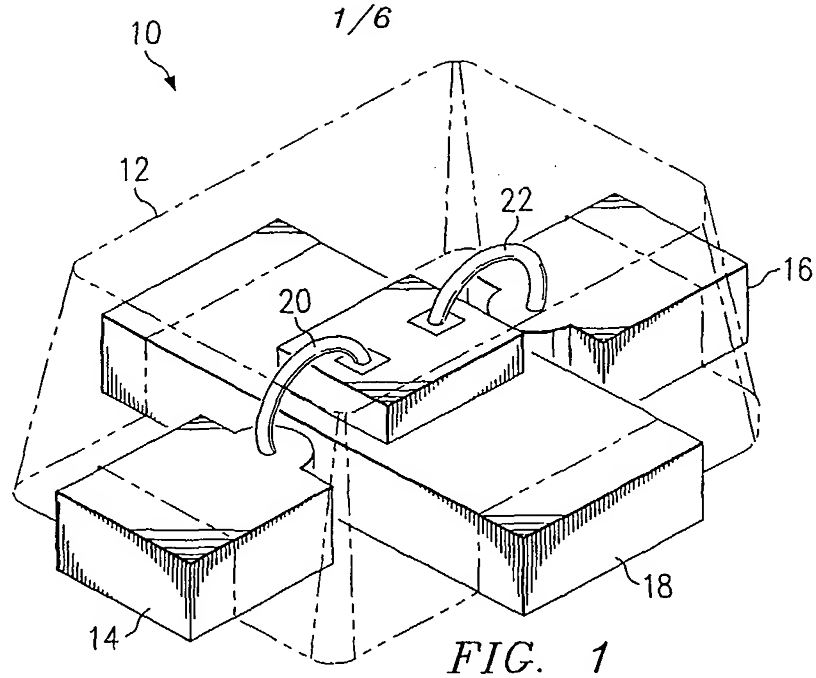

FIG. 1

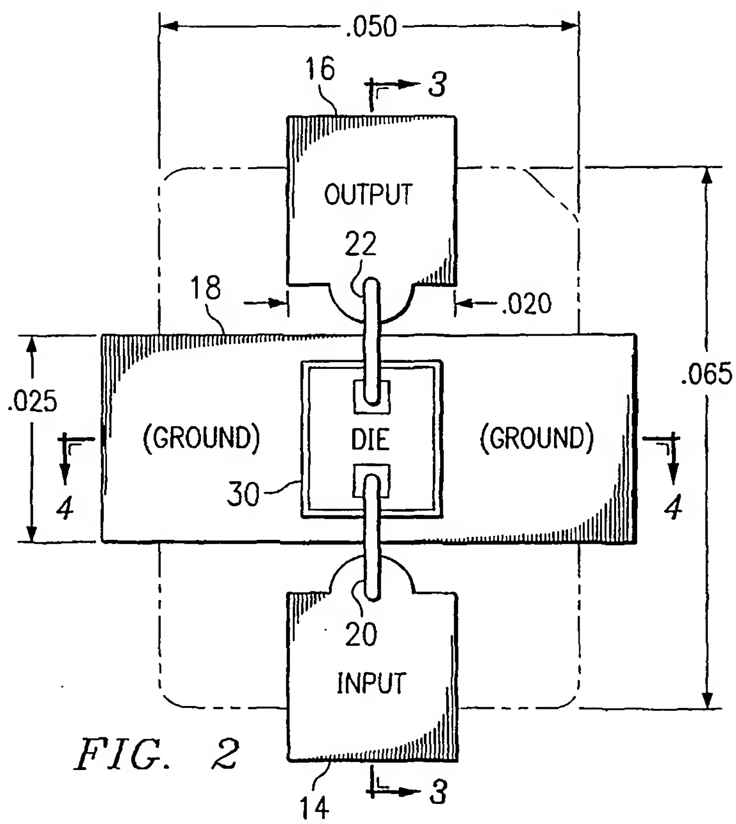

FIG. 2

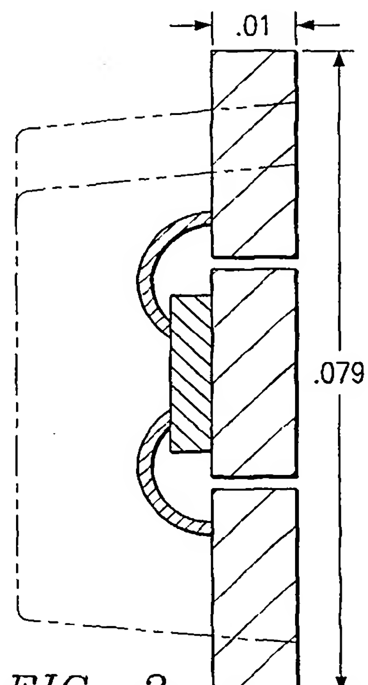

FIG. 3

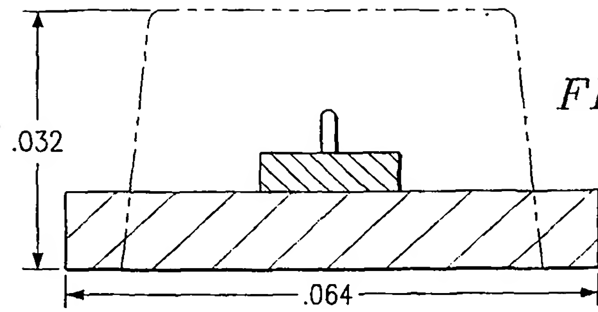

FIG. 4

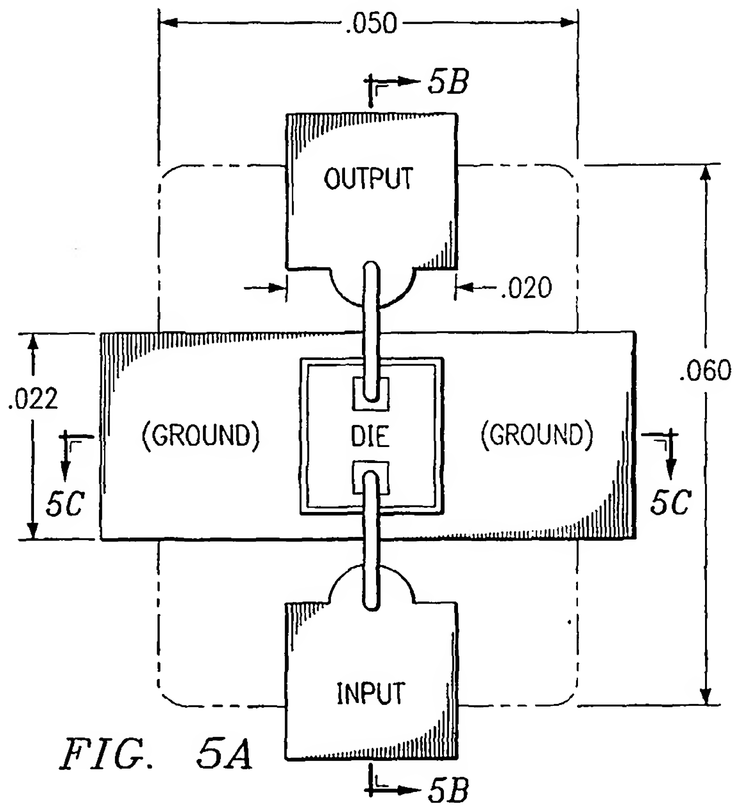

FIG. 5A

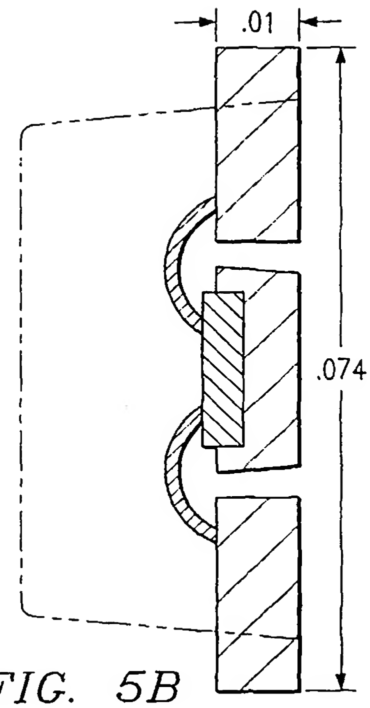

FIG. 5B

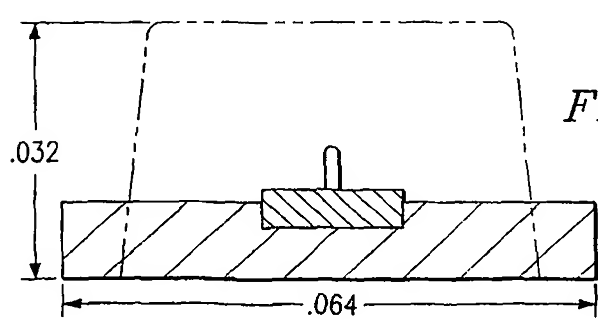

FIG. 5C

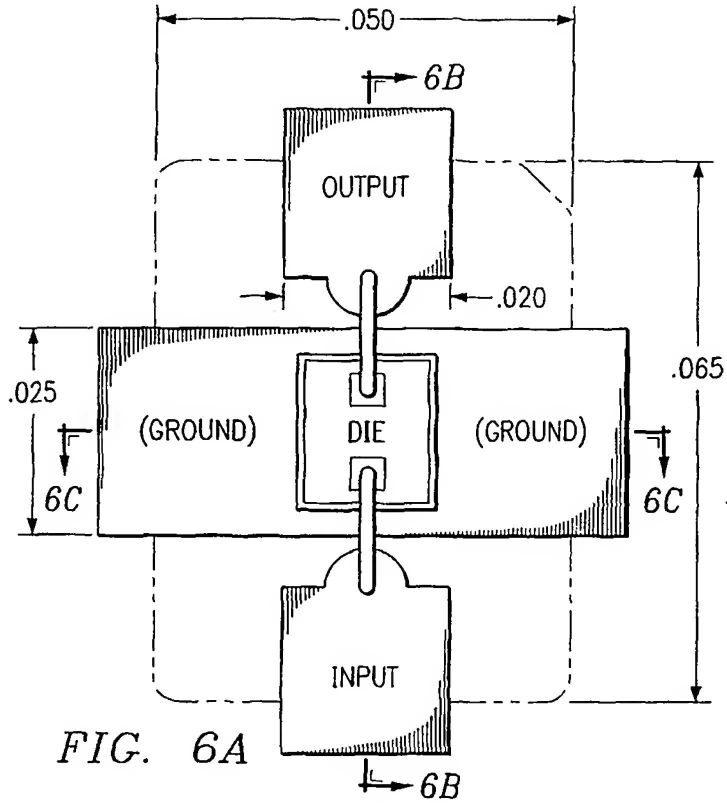

FIG. 6A

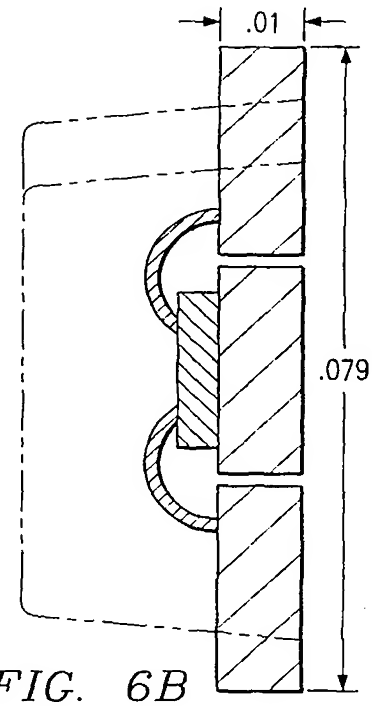

FIG. 6B

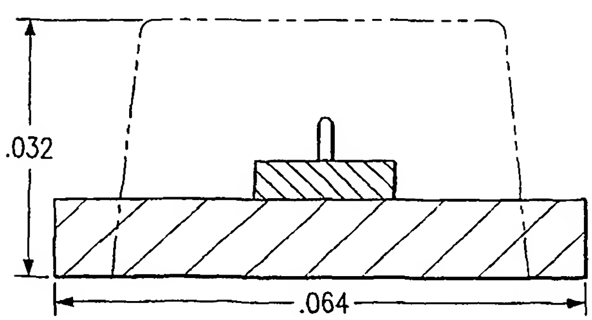

FIG. 6C

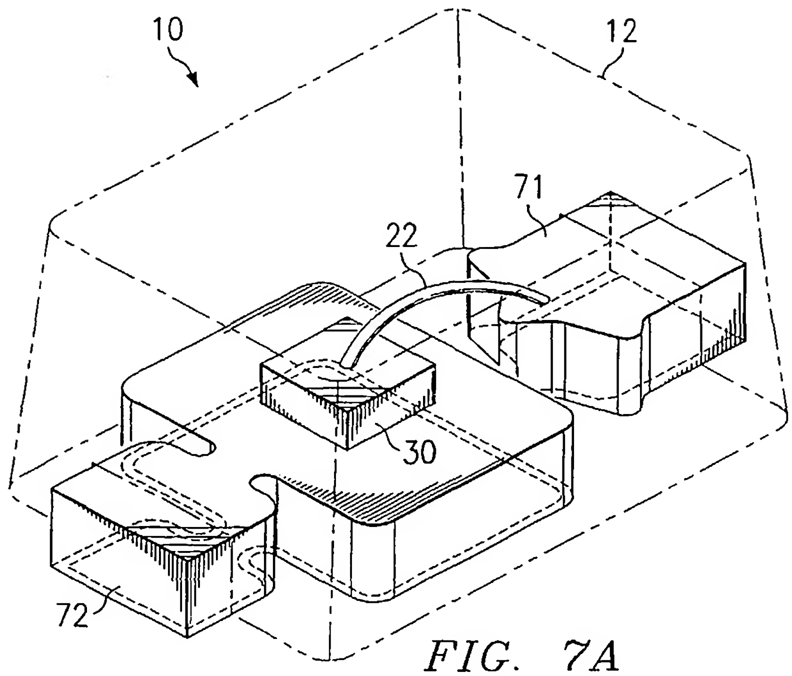

FIG. 7A

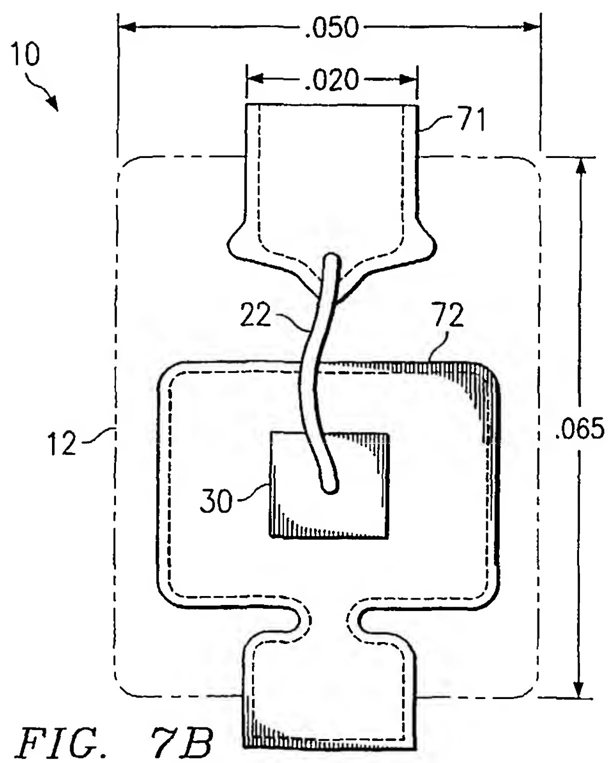

FIG. 7B

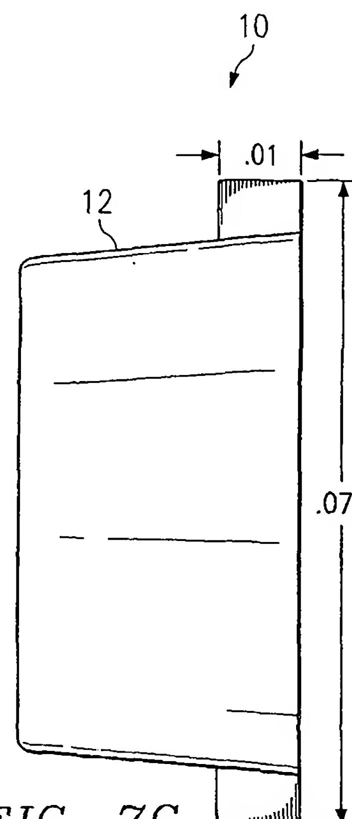

FIG. 7C

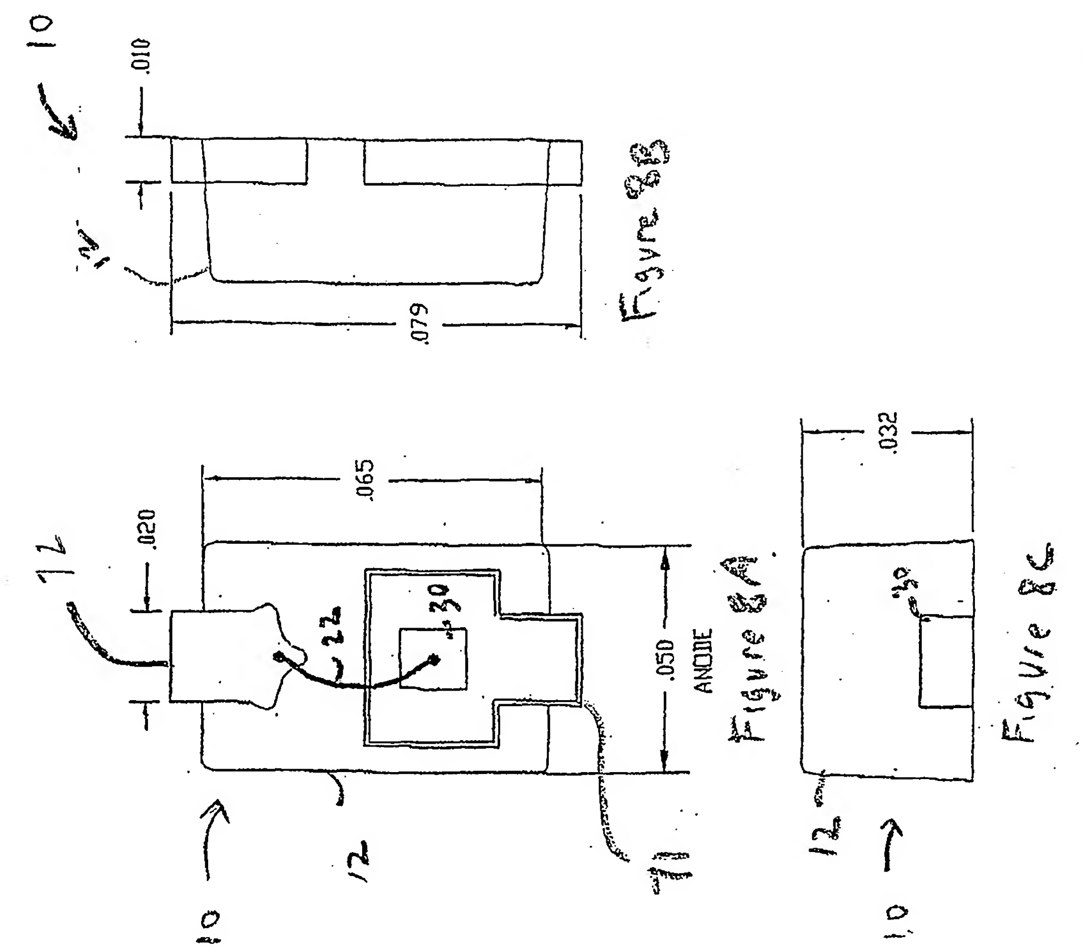

Figure 8A, 8B, 8C

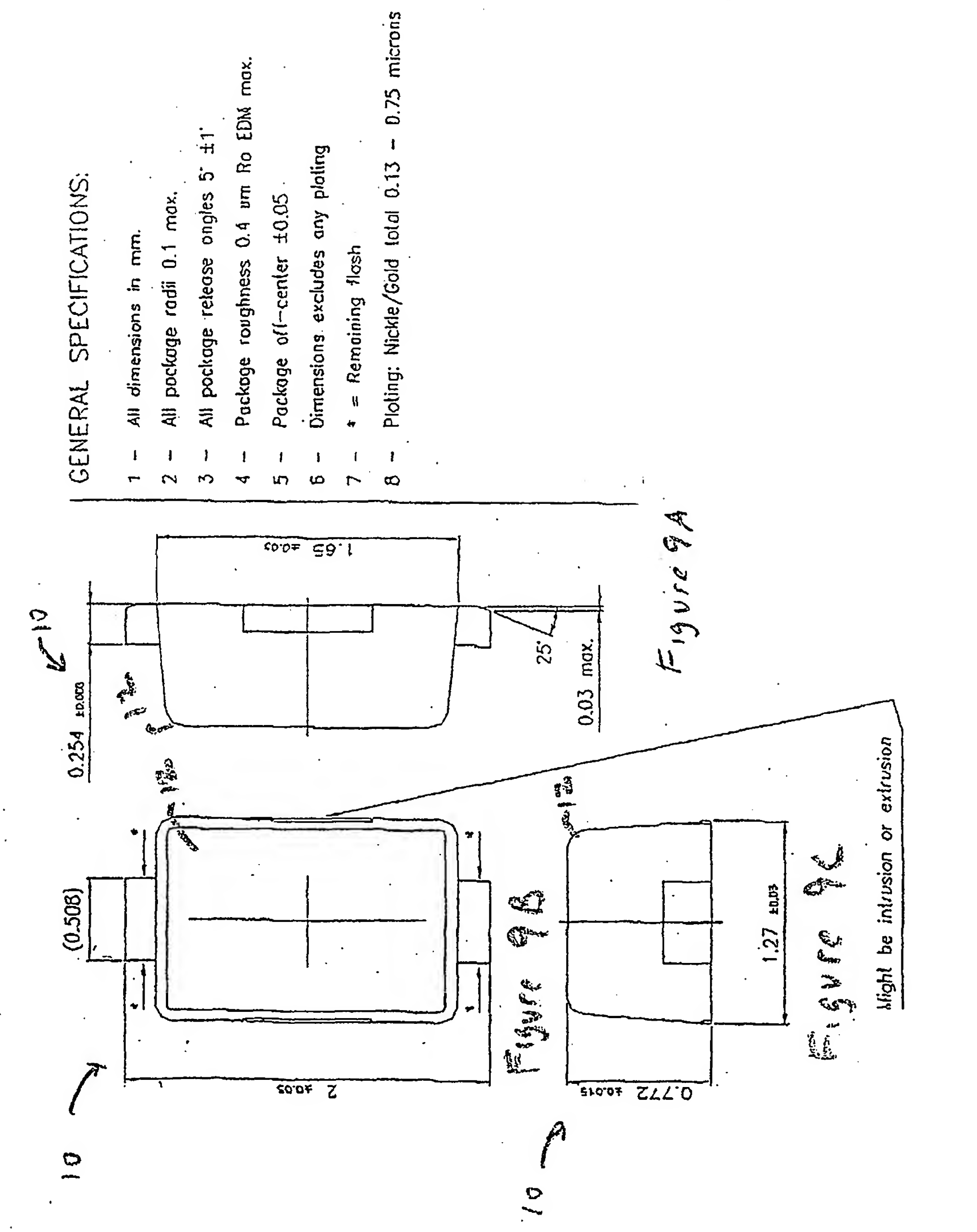

Figure 9A, 9b, 9C